

RESPONSE UNDER 37 C.F.R. § 1.116  
EXPEDITED PROCEDURE  
EXAMINING GROUP 2814

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicant(s):** Steven J. Koester

**Examiner:** Anh D. Mai

**Serial No:** 10/717,279

**Art Unit:** 2814

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**For:** SEMICONDUCTOR FIELD-EFFECT  
TRANSISTOR HAVING STRAINED-LAYER

**Dated:** June 2, 2009

**Confirm. No:** 7401

Commissioner of Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

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Sir:

In response to the Final Office Action dated April 17, 2009, Applicants submit the following remarks for entry of record in the above-identified patent application.

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**CERTIFICATE OF ELECTRONIC FILING**

I hereby certify that this correspondence is being deposited with the United States Patent & Trademark Office via Electronic Filing through the United States Patent and Trademark Office e-business website, on June 2, 2009.

Dated: June 2, 2009

  
Harry Andrew Hild Jr.